Novel CCII-based Field Programmable Analog Array and its Application to a Sixth-order Butterworth LPF

Soliman A. Mahmoud[*1], Eman A. Soliman[2]

[*1]Electrical and Computer Engineering Dept., Sharjah University, Sharjah University City, Sharjah, Postcode27272, UAE, [2]Electrical and Electronics Engineering Dept., The German University in Cairo, New Cairo City, Main Entrance Al Tagamoa Al Khames,Cairo, Postcode 11835, Egypt

[*1]solimanm@sharjah.ac.ae; [2]eman.azab@guc.edu.eg

Abstract

In this paper, a field programmable analog array (FPAA) is proposed. The proposed FPAA consists of seven configurable analog blocks (CABs) arranged in a hexagonal lattice such that the CABs are directly connected to each other. This structure improves the overall frequency response of the chip by decreasing the parasitic capacitances in the signal path. The CABs of the FPAA are based on a novel fully differential digitally programmable current conveyor (DPCCII). The programmability of the DPCCII is achieved using digitally controlled three-bit MOS ladder current division network. No extra biasing circuit is required to generate specific analog control voltage signals. The DPCCII has constant standby power consumption, offset voltage, bandwidth and harmonic distortions over all its programming range. A sixth-order Butterworth tunable LPF suitable for WLAN/WiMAX receivers is realized on the proposed FPAA. The filter power consumption is 5.4mW from 1V supply; and its cutoff frequency is tuned from 5.2 MHz to 16.9 MHz. All the circuits are realized using 90nm CMOS technology from TSMC. All simulations are carried out using Cadence.

Keywords

Current Division Network; Digitally Programmable Current Conveyor; Field Programmable Analog Array; Tunable WLAN/ WiMAX Receivers

Introduction

Field programmable analog array (FPAA) is a reconfigurable hardware platform used for analog circuits design verification. The FPAA chip can be used to realize different analog circuits such as continuous time filters, variable gain amplifiers, oscillators etc [1]. The FPAA is an array of Configurable Analog Blocks (CABs) connected together. The CAB is implemented using an analog active circuit like voltage op-amp [2], Operational Trans-conductance Amplifier (OTA) [1] or Current Conveyor (CC) [3]. These circuits can be designed with programmable or constant characteristics. The CABs are connected together using an interconnecting network so that the voltage and current signals are able to propagate from one CAB to another inside the chip [1-4]. FPAA is a perfect candidate to realize multi-standard receiver like WLAN/WiMAX. This is attributed to the fact that the chip can realize filters and amplifiers with tunable specs. However; the linearity and power consumption of the receiver will depend solely on the basic active circuit used inside the FPAA.

Current conveyors (CCs) are considered to be excellent candidate active circuit for the FPAA. CCs suitable for high frequency voltage mode applications are introduced in [5-6]. The second generation current conveyor (CCII) is a three terminal active circuit named Y, X and Z. A unity gain voltage and current mode amplifiers are realized between Y-X and X-Z terminals respectively for the CCII. A programmable versions of the CCII has been given in [7-8] by introducing a digitally controlled programmable current factor between X and Z terminals. The DPCCII circuit symbol is shown in Fig.1 and its terminal characteristics are given by equation (1).

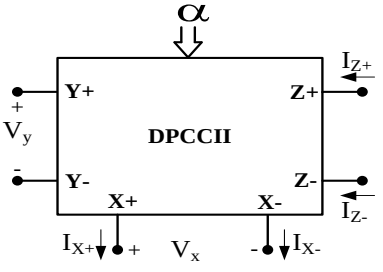

FIG. 1 DPCCII CIRCUIT SYMBOL

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \alpha & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (1)$$

Where 'α' ($0 \leq \alpha \leq 1$) is a digitally programmable gain factor.

The DPCCII circuit in [8] programmed the current between X and Z using CMOS current division network (CDN). However; the used CDN needed extra circuitry to generate variable biasing voltages to ensure that all the circuit transistors were in the saturation mode and this feature will increase significantly the hardware complexity of the proposed FPAA.

In this paper, a novel realization of a fully differential DPCCII is presented using a different CDN that doesn't need external biasing circuit. The DPCCII is tuned by means of three-bit digital control codeword. The proposed DPCCII has constant standby power consumption, offset voltage, bandwidth and linearity all over its programming range. The DPCCII is used as the basic circuit for a hexagonal FPAA. The FPAA is digitally controlled and no interconnection network is used for signal routing to increase the chip efficiency. The FPAA is used to realize a sixth-order Butterworth tunable LPF for WLAN/WiMAX receivers. The paper is organized as follows; section II the proposed DPCCII based FPAA is given, section III the proposed DPCCII realization is proposed, in section IV a sixth-order LPF is realized using the proposed FPAA, and finally the paper is concluded in section V.

Proposed Realization of DPCCII Based FPAA

The proposed FPAA consists of seven CABs based on the DPCCII. The DPCCII operates as a voltage mode active circuit by connecting X and Z terminals to resistive loads so that the Y and Z terminals are used as the input terminal and the output terminal respectively. The main advantage of the proposed DPCCII is that it can be turned off by setting the parameter 'α' to zero using the code word '000'. Thus; no programmable switches exist between the different CABs. As the CAB can be turned on/off via the MOS switches of the CDN existing inside the DPCCII.

The proposed FPAA consists of seven CABs arranged in a hexagonal lattice such that the CABs are directly connected to each other. This structure eliminates the need to global interconnection wires in the FPAA; which improves the overall frequency response of the chip by decreasing the parasitic capacitances in the signal path. This can be achieved as long as the outputs of the circuits used inside the CAB can be set to null. Removing the interconnection network that was implemented using switches in previous designs [1-4] improved the frequency response of the chip because it reduced the total parasitic capacitance in the signal path.

The FPAA architecture is shown in Fig.2. The six CABs at the edges of the FPAA consist of three DPCCIIs while the CAB at the center consists of six DPCCIIs. The CABs located at the edges of the FPAA contains three DPCCII named 'A, B, and C'. For simplicity; single ended DPCCIIs are drawn inside the CABs as shown in Fig. 2. At the center of each CAB, a differential port is used as an input voltage port or as an output current port. This differential port is connected to the Y terminal of the DPCCIIs inside each CAB. As for the Z terminal of the DPCCIIs inside the CAB, each one of them is connected to the differential port located at the center of another neighboring CAB.

To realize active filters on FPAA, negative feedback connections are required to be able to realize different filter responses. Thus, circuit 'C' output is connected in a negative form to provide negative feedback. As for the centered CAB; it consists of six DPCCIIs 'A, B, C, D, E and F'. Their Y ports are connected to the differential port at the center of the CAB while their Z ports are connected to another adjacent CAB's differential port.

The proposed FPAA can be used also to realize different voltage mode analog signal processing applications; simply by connecting the X and Z terminals to resistive/capacitive loads. The summed current at the differential port of each CAB can be used as the FPAA output current signal. According to the load connected at the output port, different analog signal processing application can be realized such as VGAs, integrators, filters etc.

Choosing the passive loads to be placed off chip will save a tremendous area and will not lead to increase the number of the chip I/O pins. The implementation of the loads leaves optional to the FPAA user; whether the loads are made programmable or constant. The proposed FPAA chip is composed of seven CABs. Each CAB has one differential I/O port for voltage mode applications 'Y and Z'. Thus the chip has a total of 14 I/O pins. The DPCCIIs inside the CABs are programmed using shift registers (SR) and inverters. Each DPCCII is programmed using a three bit

codeword and its complement. A serial 9-bit SR is used to program the edged CABs and an 18-bit SR is used for the centered CAB. This control method adds 7 pins to the FPAA chip.

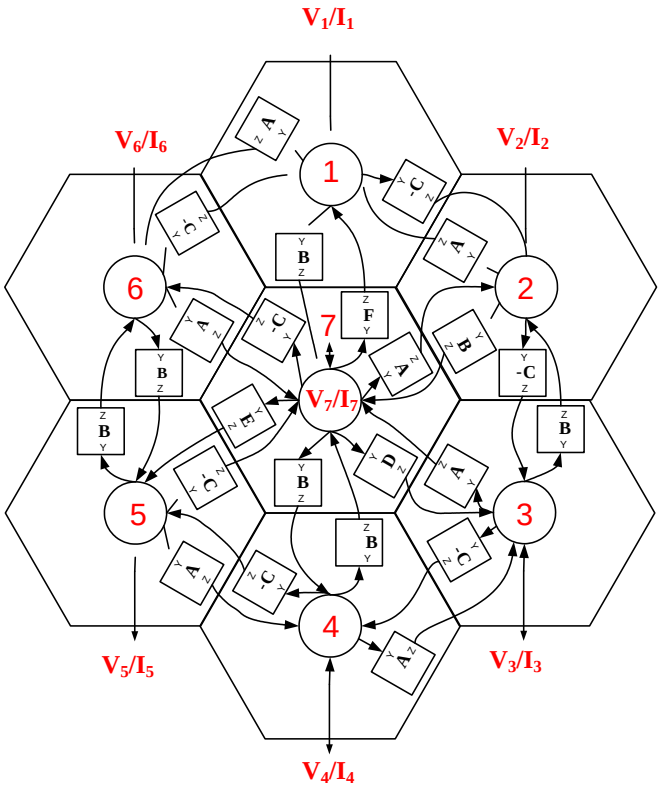

FIG. 2 PROPOSED DPCCII BASED FPAA ARCHITECTURE

Proposed Realization of DPCCII

Review of Programmable Current Conveyors

Many single ended and fully differential realizations for the CCII were proposed [5-6]. The CCII can be realized by cascading a voltage follower and a current follower to achieve the required I-V characteristics. To design a programmable CCII; two approaches were used. The first approach is using current mirrors to scale the current at the Z port [7]. However; this method suffers from transistor mismatching problems. The second one is using a current division network (CDN) added in cascade with the current follower. Thus; the Z port current becomes a scaled copy of the X port current [8].

The CDN consists of a number 'n' of current division cells connected in cascade. Each cell divides the current flowing into two halves. One half goes to the next cell and the other half flows into one of two parallel MOS switches controlled using a digital bit and its complement. Finally, all the currents of the cells controlled using the bits 'a_n' are added together to give the CDN's first output current 'I_{o1}'; while the switches controlled using '$\overline{a_n}$' and the last cell current are added to give the CDN's second output current 'I_{o2}'. The values of the CDN output currents and the current programming factor are given as follows:

$$I_{o1} = \alpha I_{in} \quad (2)$$

$$I_{o2} = (1-\alpha) I_{in} \quad (3)$$

$$\alpha = \frac{1}{2^n} \sum_{i=0}^{n} 2^i a_i \quad (4)$$

The current division factor 'α' changes with the digital codeword applied to the CDN 'a_{n-0}'. The CDN used in [8] was based on differential amplifiers (DAs) biased using constant current sources; if the CDN input current is injected at the DAs sources while their gate voltages are the same, then the input current will be divided equally between the DAs transistors. The main disadvantages of the CDN in [8] are the use of current sources which increased the circuit power consumption. In addition, the DAs gate voltages must be tuned with every codeword to ensure that the DAs would stay in the saturation region. In the following subsection, a newly proposed digitally programmable CCII (DPCCII) is realized using two fully differential CCIIs and three-bit MOS ladder CDNs given in [9].

Novel DPCCII Realization

The proposed DPCCII block diagram is shown in Fig. 3. The circuit consists of two fully differential CCII and two three-bit MOS ladder CDNs. The first CCII conveys the differential voltage applied to the Y port to the X port and then converts it to a current using a grounded resistor 'R'. Then; the X port current is conveyed to the Z port. This current flows into a three-bit MOS ladder CDN. The current division factor changes with the digital codeword applied to the CDN '$a_2a_1a_0$'.

The CDN which consisting of only MOS transistors operated as resistors and switches at the same time, is shown in Fig.4. In this CDN; the current division principle depends on the fact that the value of the equivalent resistance seen at each cell output node -the one connected to the next cell and the one to the switches- is equal irrespective of the MOS transistors DC operating mode. This can be achieved only when the output current nodes 'I_{o1}' and 'I_{o2}' potentials are set to zero [7]. Thus; another grounded Y port CCII is

used such that its X port is connected to the CDN first output node to satisfy the virtual ground condition at the CDN outputs. This X port differential current is conveyed to the Z port current such that the relation between the differential voltage of Y port and the Z port differential current is given by equation (5). The CCII circuit used for this proposed realization is given in [10].

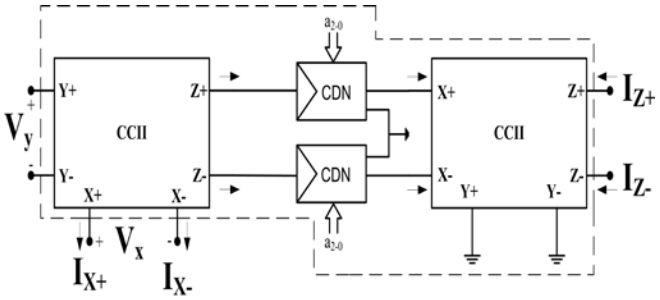

FIG. 3 PROPOSED DPCCII BLOCK DIAGRAM

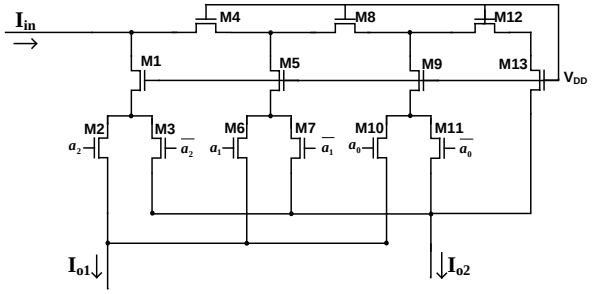

FIG. 4 CIRCUIT DIAGRAM OF A THREE-BIT MOS CDN

$$I_z = \alpha I_x = \frac{\alpha}{R} V_y \qquad (5)$$

The CCII used is shown in Fig.5. The circuit consists of two differential amplifiers (DAs) composed of M1-M2 and M3-M4. One transistor from each DA is connected to the highest supply and the other transistor is connected to a constant current source M5-M6. The two DAs are biased using current sources formed with M7-M8. The voltage following action is carried out by forcing the two DAs to have the same differential and common mode currents. The current following action is done through the class AB output stages M11-M12, M20-M21 and M15-M16, M22-M23. The standby current of the output stage is controlled via transistors M9-M10, M13-M14 and M17-19. The circuit was proposed in [10]. Since in this work the CCII is used in a hierarchal structure; it is necessary to control the common mode value of the output terminal. Thus, two transistors are used for that purpose M24-M25. A classical common mode feedback circuit is used to generate the voltage signal 'V_{CMFB}' to adjust the output voltage value.

The DPCCII is realized and simulated using 90nm TSMC CMOS technology model under balanced supply voltage of ±0.5V with Virtuoso. The DPCCII is tested while varying the codeword '$a_2a_1a_0$'. The digital bit '1' and '0' is given by 0.5V and -0.5V respectively. The proposed DPCCII has constant standby power at 0.6mW. The voltage gain open circuit bandwidth and the current gain short circuit bandwidth are also constant at 340 MHz and 540 MHz respectively. The X terminal offset voltage and finite output resistance are less than 10mV and 49Ω respectively; they are constant for all the combinations of the codeword. The voltage conveying action between Y and X under open circuit load is shown in Fig.6 while the derivative of the programmable current conveying action between X and Z terminal under short circuit load –Y is grounded- is shown in Fig.7.

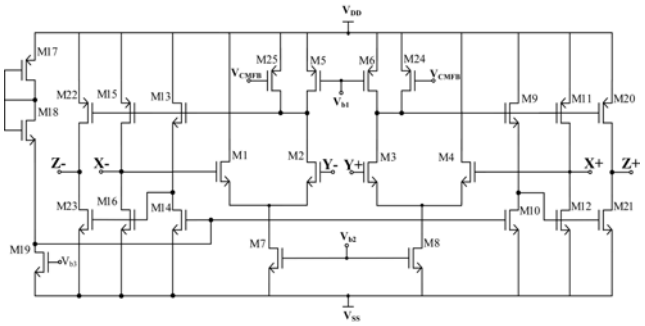

FIG. 5 CCII CIRCUIT DIAGRAM [11]

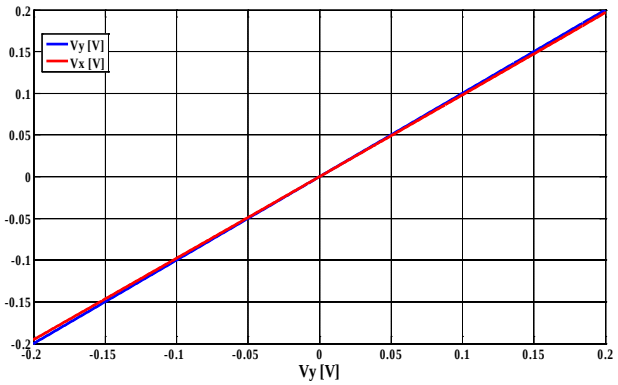

FIG. 6 VOLTAGE CONVEYING ACTION BETWEEN Y AND X TERMINALS

The voltage conveying action is achieved with range ±0.2V while the current programming is achieved over with range ±200μA. The magnitude response of the DPCCII voltage and current gains are shown in Fig. 8 and 9 respectively. The offset voltage and finite resistance at X terminal are shown in Fig. 10 and 11 respectively. The third harmonic distortion of the

voltage gain is measured at different codeword combinations. The HD_3 of the Z terminal current at Y terminal input voltage of 1 MHz and 200mVpp is measured while varying the codeword. The simulation result is given in Table I. The HD_3 of Z terminal

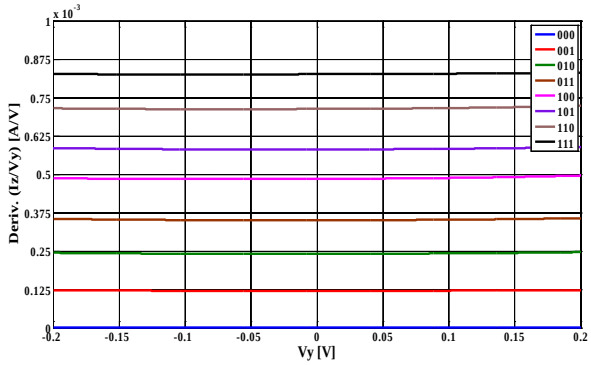

FIG. 7 DERIVATIVE THE RATIO BETWEEN THE Z TERMINAL CURRENT TO THE Y TERMINAL VOLTAGE

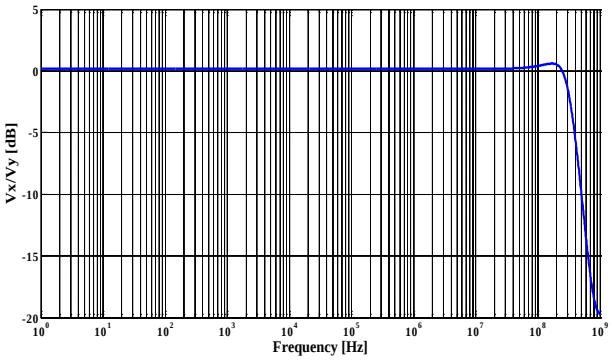

FIG. 8 MAGNITUDE RESPONSE OF THE VOLTAGE CONVEYING ACTION BETWEEN Y AND X TERMINALS

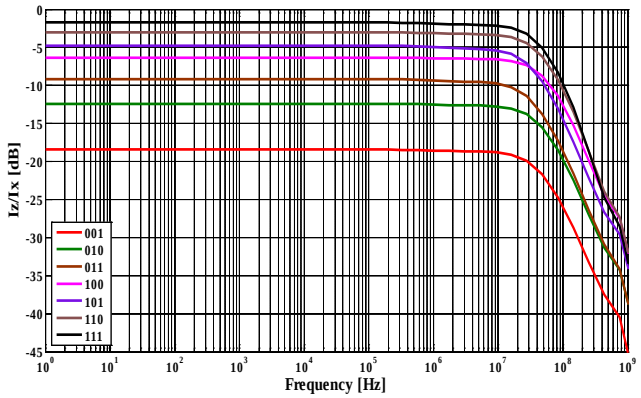

FIG. 9 MAGNITUDE RESPONSE OF THE CURRENT PROGRAMMING BETWEEN X AND Z TERMINALS

current for different codeword is less than -47.9dB. The temperature variation effect on the DPCCII Z terminal current is tested while varying the codeword. The differential current variation ranged from 107fA to 4fA as shown in Fig.12.

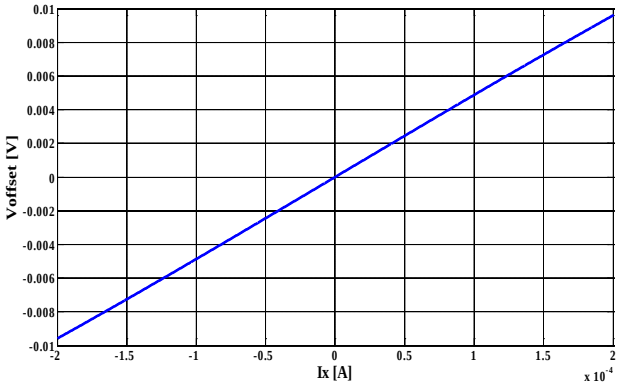

FIG. 10 OFFSET VOLTAGE AT X TERMINAL

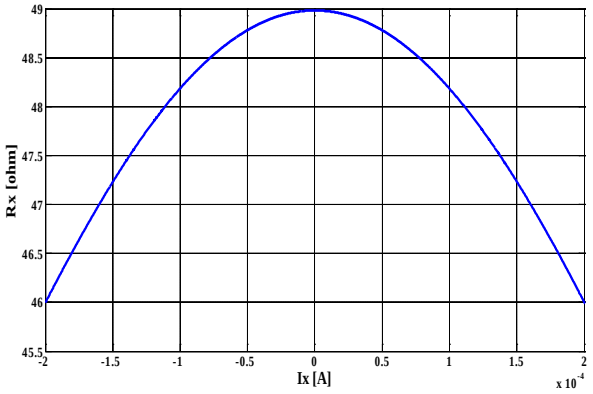

FIG. 11 FINITE RESISTANCE AT X TERMINAL

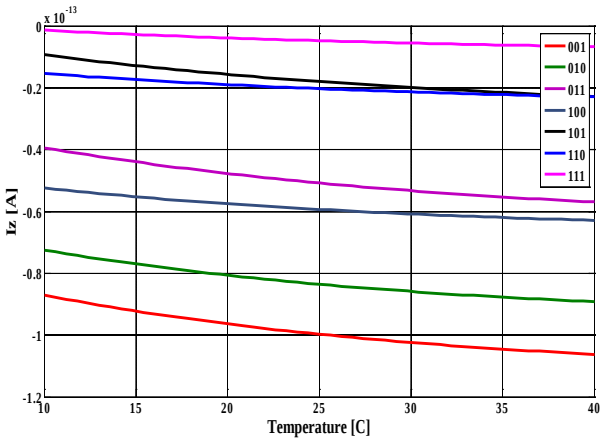

FIG. 12 DIFFERENTIAL Z CURRENT VARIATION WITH TEMPERATURE

Monte Carlo simulation is performed to test the variation in the ratio between the Z terminal differential current to the Y terminal differential voltage versus 20% mismatching and process variations as shown in Figs. 13 and 14 respectively. The value of 'α' is 0.875. As seen from the simulations the variation is very small.

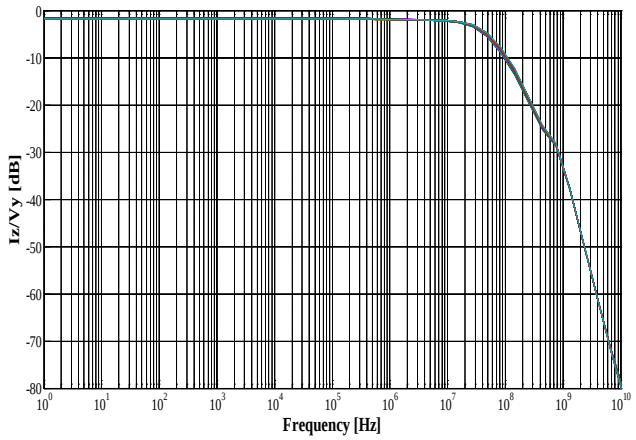

FIG. 13 RATIO BETWEEN THE DIFFERENTIAL Z CURRENT TO THE Y DIFFERENTIAL VOLTAGE VARIATION WITH RESPECT TO 20% MISMATCH ERRORS

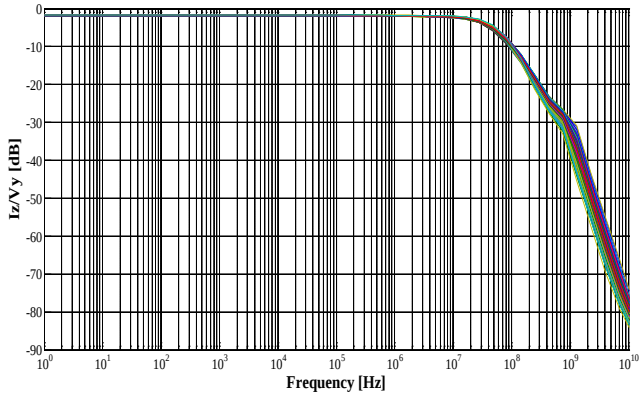

FIG. 14 RATIO BETWEEN THE DIFFERENTIAL Z CURRENT TO THE Y DIFFERENTIAL VOLTAGE VARIATION WITH RESPECT TO 20% PROCESS VARIATION

TABLE 1 THE Z TERMINAL CURRENT DIVISION FACTOR AND ITS HD_3

Codeword 'a2a1a0'	'α' Theoretical	'α' Simulated	HD_3 [dB]
000	0	5e-12	--
001	0.125	0.121	-51.8
010	0.25	0.241	-48.57
011	0.375	0.351	-47.9
100	0.5	0.485	-51.9
101	0.625	0.581	-56.9
110	0.75	0.713	-55.4
111	0.875	0.826	-61.7

Comparison between the proposed realization and the one given in [8] is presented in Table II. The power dissipation of the proposed realization is much less than the one in [8]. The 3-dB bandwidth of the proposed work is also higher. The total harmonic distortion is less than -47dB at 1MHz operating frequency with the input voltage amplitude at the 200mVpp; which is higher than the one in [8].

TABLE 2 COMPARISON BETWEEN PROPOSED DPCCII AND PREVIOUS WORK

Parameter	This Work	The Work in [8]
Technology	0.09µm	0.5µm
Power Supply	±0.5V	±1.5V
Voltage Conveying Range % from the voltage supply	40%	66.6%
Power Dissipation	0.6mW	2.7mW
THD @200mv- 1 MHz	Less than -47dB	Less than -40dB

Sixth-Order Butterworth Tunable LPF

The proposed FPAA is used to realize a sixth-order Butterworth tunable voltage mode LPF. The filter is realized using cascading technique of three second-order bi-quad sections [11]. The filter is mapped on the FPAA as shown in Fig.15. The bi-quad's transfer function, cutoff frequency, quality factor, DC gain are given by the following equations:

$$\frac{V_{out}}{V_{in}} = \frac{\dfrac{\alpha_1\alpha_2}{R_1R_2C_1C_2}}{S^2 + S\dfrac{1}{R_4C_1} + \dfrac{\alpha_2\alpha_3}{R_2R_3C_1C_2}} \quad (6)$$

$$\omega_o = \sqrt{\frac{\alpha_2\alpha_3}{R_2R_3C_1C_2}} \quad (7)$$

$$Q = R_4\sqrt{\frac{\alpha_2\alpha_3C_1}{R_2R_3C_2}} \quad (8)$$

$$\frac{V_{out}}{V_{in}}_{S=0} = \frac{\alpha_1R_3}{\alpha_3R_1} \quad (9)$$

The WLAN/WiMAX receiver cutoff frequency ranges from 8.1 MHz to 13.5 MHz. The proposed filter's cutoff frequency can be tuned by varying 'α_2' however the filter's quality factor will vary too. Consider the

following selection of the design parameters: $R_1=R_2=R_3=R_4=R$, $C_2=3C_1$, $\alpha_1=\alpha_3=0.875$.

The input voltage is at CAB1 and the output is taken from CAB2. The second-order sections are mapped to circuits 'B1, C7, A6', 'B6, A5, C4' and 'A4, B3, C2'. The resistors R are the ones connected to the DPCCIIs X terminals. The FPAA is simulated with the filter mapped on it with the following values for R, C_1 and C_2 selected as 1.1kΩ, 2pF and 6pF respectively. The current programming factor 'α_1', 'α_2' and 'α_3' are the ones for circuits 'B1, B6, A4', ' C7, A5, B3' and 'A6, C4, C2' respectively. The tuning of the cutoff frequency is done by varying 'α_2'. The value of 'α_1 and α_3'are selected at 0.875 to give DC gain 0dB. The magnitude response of the filter is shown in Fig. 16. Summary of the filter's simulation results is given in Table III. The output referred to noise density at the filter's cutoff frequency is measured.

Conclusion

A newly proposed FPAA is introduced. The proposed FPAA can be used to realize high frequency applications because no interconnecting network is used. The FPAA consists of seven CABs arranged in a hexagonal lattice. The CABs are realized using digitally controlled fully differential current conveyor (DPCCII) with total standby power of 14.4mW. The DPCCII circuit has constant standby power of 0.6mW, bandwidth of 100 MHz, offset voltage of 2mV at 500μA, THD less than -47dB at 200mVpp and 1 MHz all over its tuning range. The FPAA is used to realize a sixth-order tunable Butterworth LPF for WLAN/ WiMAX receivers. The filter's cut-off frequency is tuned from 5.2 MHz to 16.9 MHz.

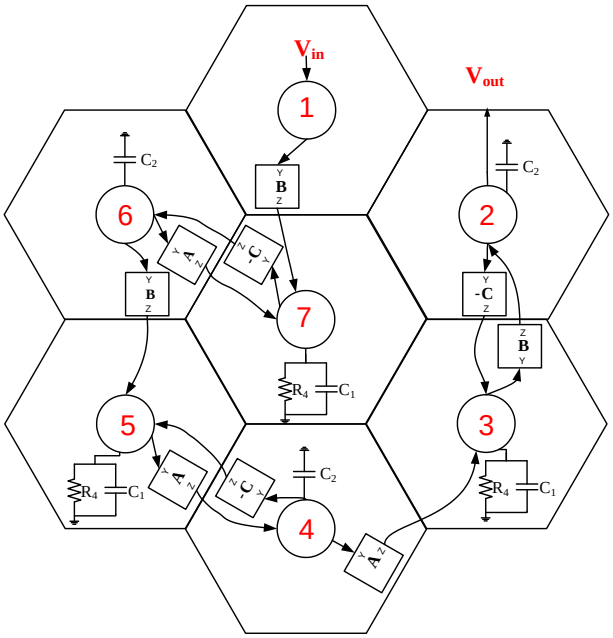

FIG. 15 SIXTH-ORDER DPCCII BASED LPF MAPPED ON THE FPAA

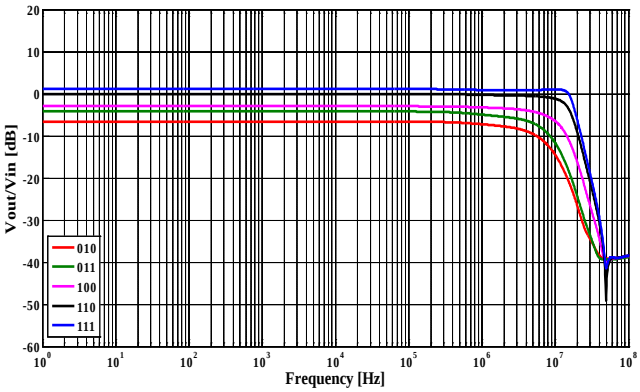

FIG. 16 MAGNITUDE RESPONSE OF THE SIXTH-ORDER TUNABLE LPF

TABLE 3 PROPOSED FILTER SIMULATION RESULTS

Codeword 'a2a1a0'	f_o [MHz]	DC gain [dB]	Noise [nV/√Hz]
010	5.2	-6.6	108
011	6.2	-4.1	141
100	8.5	-3	100
110	13.9	0	104
111	16.9	1.2	100

REFERENCES

Bult, K. and Geelen, G. J. G. M., An inherently linear and compact MOST-only current division technique, *IEEE J. Solid-State Circuits* **27** (1992), pp. 1730-1735.

Gaudet, V. C. and Gulak, P. G., CMOS implementation of a current conveyor-based field-programmable analog array, *Conference of Signals, Systems and Computers* **2** (1997), pp. 1156.

Hassan, T.M. and Mahmoud, S.A., Fully Programmable Universal Filter with Independent Gain-ωo-Q Control Based On New Digitally Programmable CMOS CCII, *Journal of Circuits, Systems and Computers* **18** (2009), pp. 875-897.

Looby, C. A. and Lyden, C., Op-amp based CMOS field-programmable analogue array, *Proc. Of IEE Circuits, Devices and Systems* **147** (2000), pp. 93-95.

Mahmoud, S. A., Digitally Controlled CMOS Balanced Output Transconductor and Application to Variable Gain Amplifier and Gm-C Filter on Field Programmable

Analog Array, *Journal of Circuits, Systems and Computers* **14** (2005), pp. 667-684.

Mahmoud, S. A., and Awad, I. A., Fully Differential CMOS Current Feedback Operational Amplifier, *Analog Integrated Circuits and Signal Processing* **43** (2005), pp. 61–69.

Mahmoud, S. A., Hashiesh, M. A. and Soliman, A. M., Low-Voltage Digitally Controlled Fully Differential Current Conveyor, *IEEE Trans. on Circuits and Systems I* **52** (2005), pp. 2055-2064.

Mahmoud, S. A., and Soliman, E. A., Low Voltage Current Conveyor based Field Programmable Analog Arrays, *Journal of Circuits, Systems, and Computers* **20** (2011), pp. 1677-1701.

Sedra, A. and Smith, K. C., A Second-generation Current Conveyor and its Applications, *IEEE Trans. on Circuit Theory* **17** (1970), pp. 132-134.

Smith, K. C. and Sedra, A., The Current Conveyor-A New Circuit Building Block, *Proc. Of the IEEE* **56** (1968), pp. 1368-1369.

Oskooei, M. S., Masoumi, N., Kamarei, M., and Sjöland, H., A CMOS 4.35-mW +22-dBm IIP3 Continuously Tunable Channel Select Filter for WLAN/WiMAX Receivers, *IEEE J. Solid-State Circuits* **46** (2011), pp. 1382-1391.

Soliman A. Mahmoud was born in Cairo, Egypt, in 1971. He received the BSc degree with honours in 1994, the MSc degree in 1996, and the PhD degree in 1999, all from the Electronics and Communications Department, Cairo University, Egypt.

In 2005, He was decorated with the Science Prize in Advanced Engineering Technology from the Academy of Scientific Research and Technology. He was a visiting scholar at ULM University, Germany (summer 2008 and summer 2009). From September 2008- January 2010, Prof. Mahmoud served as Professor and Chairman of Electronics and Communications Engineering Department, Fayoum University, Fayoum, Egypt. He is currently on leave from Fayoum University and working at University Of Sharjah.

Prof. Mahmoud is the author and co-author of more than 100 papers in international journals and conferences. He is also author of a book titled *Design of The Differential Difference Operational Floating Amplifier*, with ISBN 978-3-639-17849-4, VDM publisher. His research and teaching interests are in circuit theory, fully-integrated analog filters, high-frequency transconductance amplifiers, low-voltage analog CMOS circuit design, current-mode analog signal processing, and mixed analog/digital programmable analog blocks.

Prof. Mahmoud is IEEE senior member. In April 2012, Prof. Mahmoud received the University of Sharjah research award for his work on 2011-2012.

Eman A. Soliman was born in Cairo, Egypt in 1984. She received the B.Sc. degree with honors in 2006 from the Electronics and Communications Department, Cairo University, Egypt, the M.Sc. degree in 2008 and the PhD degree in 2012 from the Electrical and Electronics Department, The German University in Cairo, Egypt. She is currently Assistant Lecturer in the Electrical and Electronic Department, The German University in Cairo, Cairo, Egypt. Her research interests are in circuit theory; low-voltage analog CMOS circuit design, current-mode analog signal processing, and mixed/digital applications on field programmable gate arrays.